#31/C
7-14-03
RJ

PATENT DOCKET NO. 5231.03-4000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit: 2183

Examiner: Richard Ellis

Serial No.: 09/385,394

Filed: August 30, 1999

Applicant(s): John S. Yates, Jr., et al.

Title: COMPUTER WITH TWO EXECUTION MODES

I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on June 30, 2003 as First Class Mail in an envelope with sufficient postage addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

David E. Boody

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE ACCOMPANYING RCE

Kindly amend the application as follows.

In the claims:

C1

1. (twice amended) A computer, comprising:

a processor pipeline designed to alternately execute instructions coded for first and second different computer architectures or coded to implement first and second different processing conventions;

a memory for storing instructions for execution by the processor pipeline, the memory being divided into pages for management by a virtual memory manager, a single address space of the memory having first and second pages;

a memory unit designed to fetch instructions from the memory for execution by the pipeline, and to fetch stored indicator elements associated with respective memory pages of the single address space from which the instructions are to be fetched, each indicator element designed to store an indication of which of two different computer architectures and/or execution conventions under which instruction data of the associated page are to be executed